IN THE CLAIMS:

Please amend Claim 7 as follows:

Claims 1-6 (canceled).

Claim 7 (currently amended): A memory control circuit enabling a memory to be accessed from a first processing device in response to a first or a second processing request signal, and enabling the memory to be accessed from a second device in response to a third or a fourth processing request signal, comprising:

a first group of watching circuits observing whether both of the first and second processing devices request access to the memory, based on the first and second processing request signal and the third processing request signals,

a second group of watching circuits observing whether both of the first and second processing devices request access to the memory, based on the first and second processing request signals and the signal representing an observation

of the first group of watching circuits and the [[third]] fourth processing request signal,

an address generating circuit generating and outputting a first address signal in response to the first processing request signal, a second address signal in response to the second processing request signal, a third address signal in response to the third processing request signal, and a fourth address signal in response to the fourth processing request signal,

a selection circuit, which is responsive to a selection signal, outputting one of the first through fourth address signals to the memory, and

a control circuit generating the selection signal, the control circuit outputting the selection signal for selecting the first or second address signal prior to the third or fourth address signal when signals representing an observation of the first or second group of watching circuits indicate that both of the first and second processing devices request access to the memory.

Claim 8 (previously presented): A memory control circuit as claimed in claim 7, wherein the control circuit selects the first or second address signal prior to the third and fourth address signals when both of the signals representing the observations of the first and second watching circuits indicate that both of the first and second processing devices request access to the memory, and then, after the first processing device has completed to access the memory, the control circuit selects the third address signal prior to the fourth address signal.

Claim 9 (previously presented): A memory control circuit as claimed in claim 7, wherein the memory control circuit is used in a data transmitting device for sending and receiving data with an external device, the first processing device is a central processing unit incorporated in the data transmitting device, and the second processing device is the external device, which is outside the data transmitting device.

Claim 10 (previously presented): A memory control circuit as claimed in claim 8, wherein the memory control circuit is used in a data transmitting device for sending and receiving data with an external device, the first processing device is a central processing unit incorporated in the data transmitting device, and the second processing device is the external device, which is outside the data transmitting device.

Claim 11 (previously presented): A memory control circuit as claimed in claim 9, wherein the first processing request signal has a logic level that changes when the central processing unit requests access to the memory to write data, wherein the second processing request signal has a logic level that changes when the central processing unit requests access to the memory to read-out data, wherein the third processing request signal has a logic level that changes when the external device requests access to the memory to read-out data, and wherein the fourth processing request signal has logic level that changes when the external device requests access to the memory to write data.

Claim 12 (previously presented): A memory control circuit as claimed in claim 10, wherein the first processing request signal has a logic level that changes when the central processing unit requests access to the memory to write data, wherein the second processing request signal has a logic level that changes when the central processing unit requests access to the memory to read-out data, wherein the third processing request signal has a logic level that changes when the external device requests access to the memory to read-out data, and wherein the fourth processing request signal has logic level that changes when the external device requests access to the memory to write data.